Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Cancelled.)

2. (Currently Amended) ~~The pulse width modulator circuit as set forth in Claim 1,~~ A pulse width modulator circuit for generating a reference signal having a desired duty cycle comprising:

an adjustment unit including at least one storage register and a counter, the storage register being configured for storing values corresponding to the desired duty cycle at least approximately and which are set during a working cycle in the pulse width modulator circuit for generating a reference signal, and the counter setting a cycle count (Y) indicating how often a stored first value (X) is read during the working cycle (A) from the storage register, wherein the first value stored in the storage register is variable upon reaching the cycle count (Y) to store a second value (X+1) which is set for the remainder of the working cycle after the cycle count (Y) is reached; and

an adder which receives the stored first value from the storage register and changes it upon reaching the cycle count (Y) to generate a second value (X+1) which is set for the remainder of the working cycle after the cycle count (Y) is reached.

3. (Canceled).

4. (Currently Amended) The pulse width modulator circuit as set forth in ~~Claim 1~~ Claim 2, wherein the storage register has an 8 bit capacity and the counter a 3 bit capacity.

5. (Canceled).

6. (Original) A method for driving a pulse width modulator circuit comprising the steps:

- generating a pulse width control signal having a desired duty cycle,
- defining at least one first value and a second value (46, 48) corresponding at least approximately to the desired duty cycle and being output during a working cycle for generating the pulse width control signal A times in all, where A is a predefined number, and
- setting (44) a cycle count Y dictating how often the first value and how often the second value is read during the working cycle to set the desired duty cycle as a function of an average of the first and second values output during the working cycle.

7. (Original) The method as set forth in Claim 6, wherein the first value and the second value are output to a pulse width modulator (34) for generating the pulse width control signal.

8. (Previously Presented) The method as set forth in Claim 6, wherein a first value is output Y times and the second value is output (A-Y) times.

9. (Previously Presented) The method as set forth in Claim 6, wherein the first value is an integer X and the second value is an integer X+1.

10. (Original) The method as set forth in Claim 9, wherein the first value is stored in a storage register and the second value (X+1) is generated by the addition of 1 to the first value.

11. (Previously Presented) The method as set forth in Claim 6, wherein the cycle count Y is set in a counter, the first value is output (46) during each count clock until the cycle count Y is reached and the second value is output (48) during each count clock after the cycle count is reached up to the end of the working cycle A.

12. (Original) The method as set forth in Claim 11, wherein the counter is reset at the end of each working cycle (52).

13. (Previously Presented) A method for driving a power supply wherein a pulse width control signal is generated as set forth in Claim 6 and is applied to switching means (20) for generating an output current.

14. (Canceled).

15. (Previously Presented) A computer program comprising a program code for implementing the method for driving a pulse width modulator circuit comprising the steps:

- generating a pulse width control signal having a desired duty cycle,
- defining at least one first value and a second value (46, 48) corresponding at least approximately to the desired duty cycle and being output during a working cycle for generating the pulse width control signal A times in all, where A is a predetermined number, and
- setting (44) a cycle count Y dictating how often the first value and how often the second value is read during the working cycle to set the desired cycle as a function of an average of the first and second values output during the working cycle.

16. (Cancelled.)

17. (Currently Amended) ~~The power supply of Claim 16 further~~ A power supply comprising:

switching means (20);

a pulse width modulator circuit (34) for generating a reference signal having a desired duty cycle having an adjustment unit including at least one storage register and a counter, the storage register being configured for storing values corresponding to the desired duty cycle at least approximately and which are set during a working cycle in the pulse width modulator circuit for generating a reference signal, and the counter setting a cycle count (Y) indicating how often a stored first value (X) is read during the working cycle (A) from the storage register; and

an adder which receives the stored first value from the storage register and changes it upon reaching the cycle count (Y) to generate a second value (X+1) which is set for the remainder of the working cycle after the cycle count (Y) is ~~reached.~~ reached;

wherein the first value stored in the storage register is variable upon reaching the cycle count (Y) to store a second value (X+1) which is set for the remainder of the working cycle after the cycle count (Y) is reached, and

wherein the pulse width modulator circuit (34) outputs to the switching means (20) a control signal having a desired duty cycle and corresponding to the reference signal.

18. (Currently Amended) The power supply of ~~Claim 16~~ Claim 17, wherein the storage register has an 8 bit capacity and the counter a 3 bit capacity.